REMARKS

Claims 1, 3, 7-12, 15, 16, and 18 are pending and each rejected under 35 U.S.C. § 103(a) as being unpatentable over "An Electrophoretic Display, Its Properties, and Addressing," *IEEE Transactions on Electron Devices*, Vol. ED-26, No. 8, August 1979, pp.1148-1152 by Hopper et al. ("Hopper"), in view of U.S. Patent No. 6,100,951 to Oversluizen et al. ("Oversluizen"), and further in view of U.S. Patent No. 5,238,861 to Morin et al. ("Morin"). Applicants respectfully submit that the cited references do not teach or suggest all the limitations recited by independent claims 1 or 18.

As the Office action admits, on pages 3 and 4, the combination of Oversluizen and Hopper, "does not expressly teach that the transistor and the storage capacitor share a single layer of unpatterned semiconducting material situated between the respective first layers of conductive material and the respective second layers of conductive material, as recited in claim 1, or the storage capacitor comprising a layer of unpatterned semiconducting material situated between the first layer of conductive material and the second layer of conductive material, as recited in claim 18."

The Office action, however, argues that Morin, "discloses an active matrix display device ... comprising a transistor ... and a storage capacitor ... both sharing a single layer ... of unpatterned semiconducting material." Page 4. Applicants respectfully disagree.

Morin describes a series of conductive blocks (P, 12, or SP), in FIGS. 3, 4a, 4b, and 12 that form a *pattern*. See Column 3, lines 46-59. A semiconductive film 14 is then deposited on these patterned conductive blocks to form a semiconducting layer. Column 3, lines 60-63. Morin further describes that photoetching of this semiconductive layer forms patterns: "In a second photoetching, patterns are defined through a second masking level such as patterns hatched on FIG. 3 ..." Column 3, lines 64-65. In addition, FIGS. 4a, 4b, and 12, expressly show a semiconductive layer 14 that is patterned to conform with the shape of the conductive blocks (P, 12, or SP). Thus, the semiconducting layer described by Morin is a *patterned* semiconducting layer, in direct contrast to the unpatterned semiconducting layer recited by independent claim 1.

Accordingly, Hopper, Oversluizen, and Morin, even if combined, do not teach or suggest a display including a transistor and a storage capacitor that share a layer of unpatterned

semiconducting material situated between respective first layers of conductive material and respective second layers of conductive material, a limitation expressly required by claim 1.

For reasons similar to those discussed with respect to claim 1, Applicants submit that the cited references do not teach or suggest all the limitations recited by independent claim 18. In particular, Morin expressly describes a patterned semiconductive layer 14 that functions as part of the storage capacitors, as shown in FIG. 4b. Accordingly, even if Hopper, Oversluizen, and Morin can be combined, that combination will not teach all the limitations expressly recited by claim 18, such as the express limitation of a storage capacitor comprising a layer of unpatterned semiconducting material.

Therefore, independent claims 1 and 18 are patentable over Hopper in view of Oversluizen, and further in view of Morin. Because claims 3, 7-12, 15, and 16 depend either directly or indirectly from independent claim 1, and include all the limitations thereof, Applicants respectfully submit that these claims are patentable as well.

CONCLUSION

In view of the foregoing, Applicants present all pending claims for reconsideration and the withdrawal of all grounds of rejection, and allowance of claims 1, 3, 7-12, 15, 16 and 18 in due course. The Examiner is invited to contact Applicants' undersigned representative by telephone at the number listed below to discuss any outstanding issues.

Respectfully submitted,

Date: April 9, 2004
Reg. No. (Limited Recognition)

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